

FIG. 1

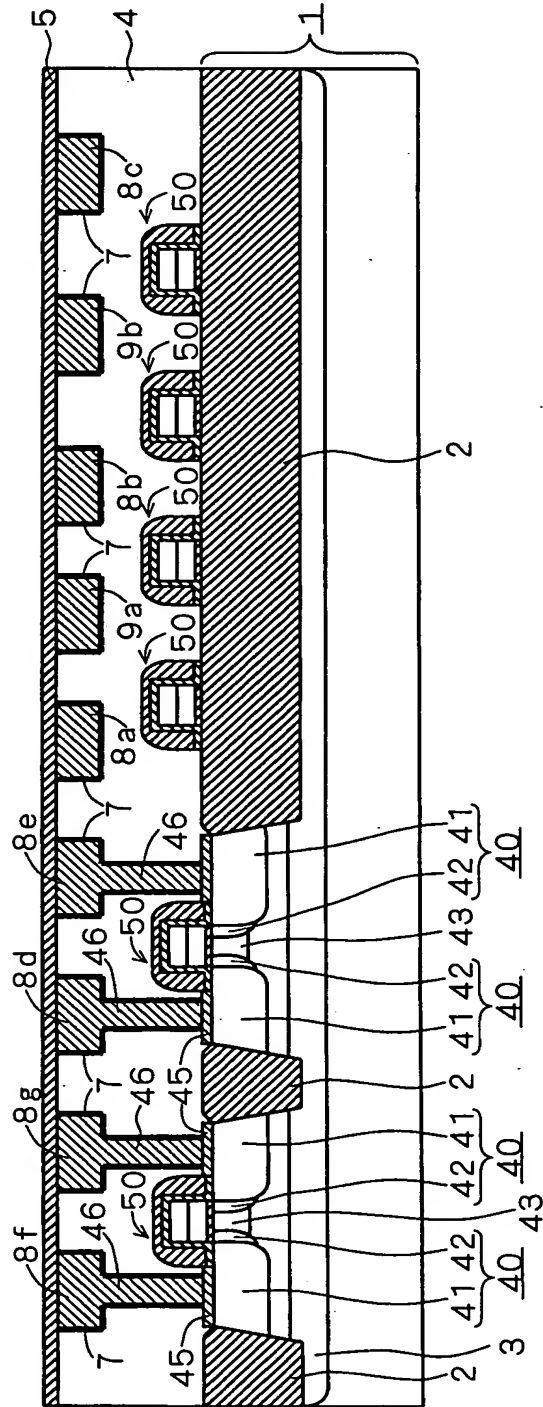


FIG. 2

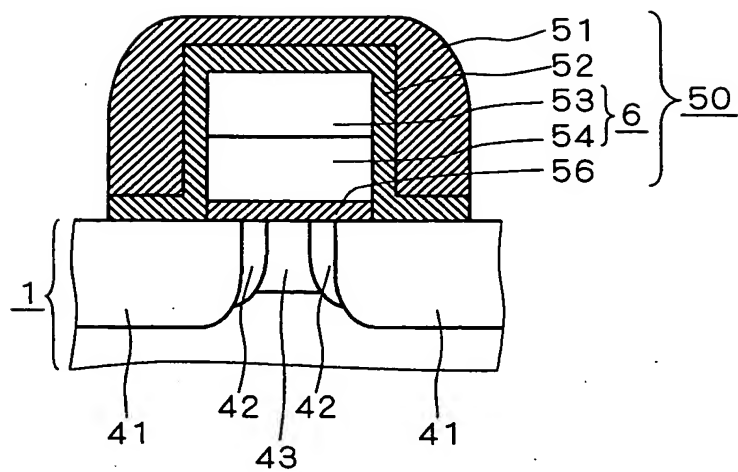


FIG. 3

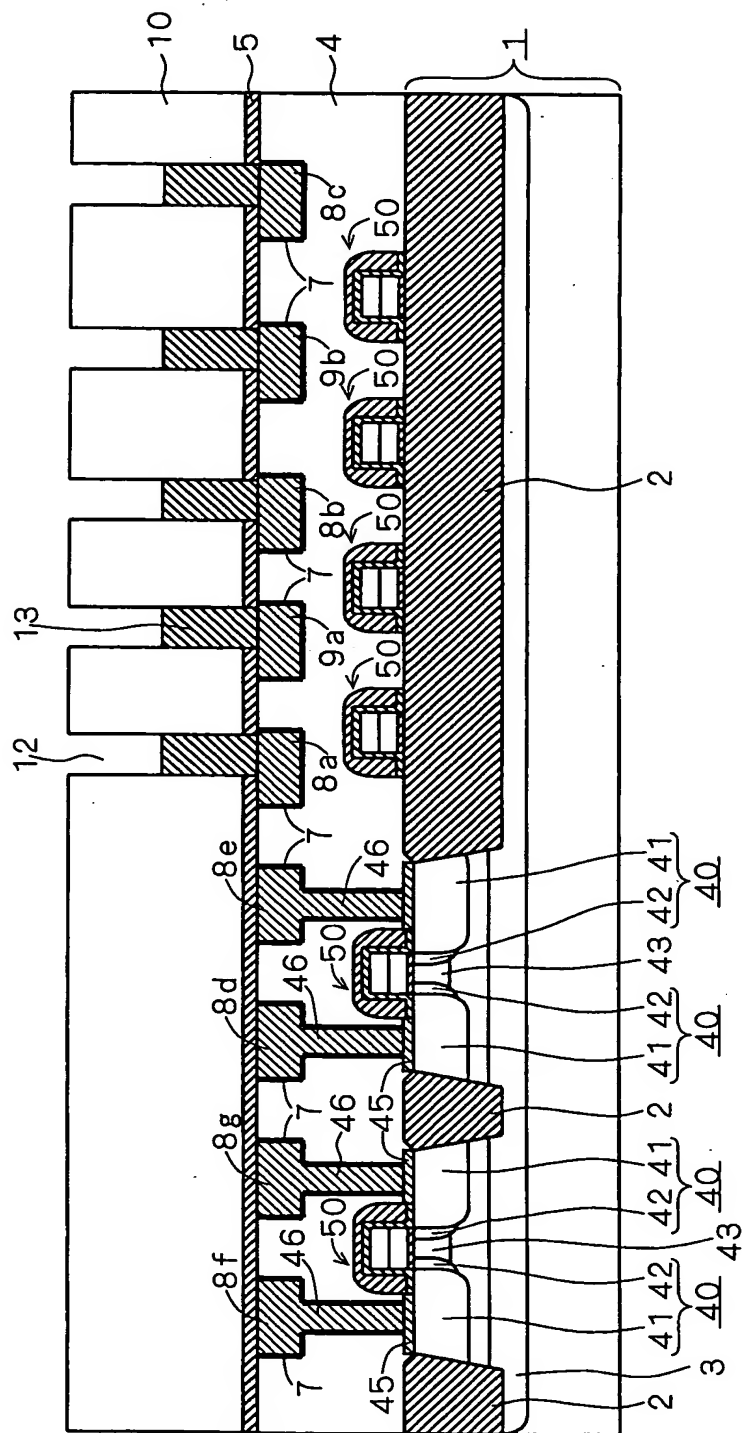
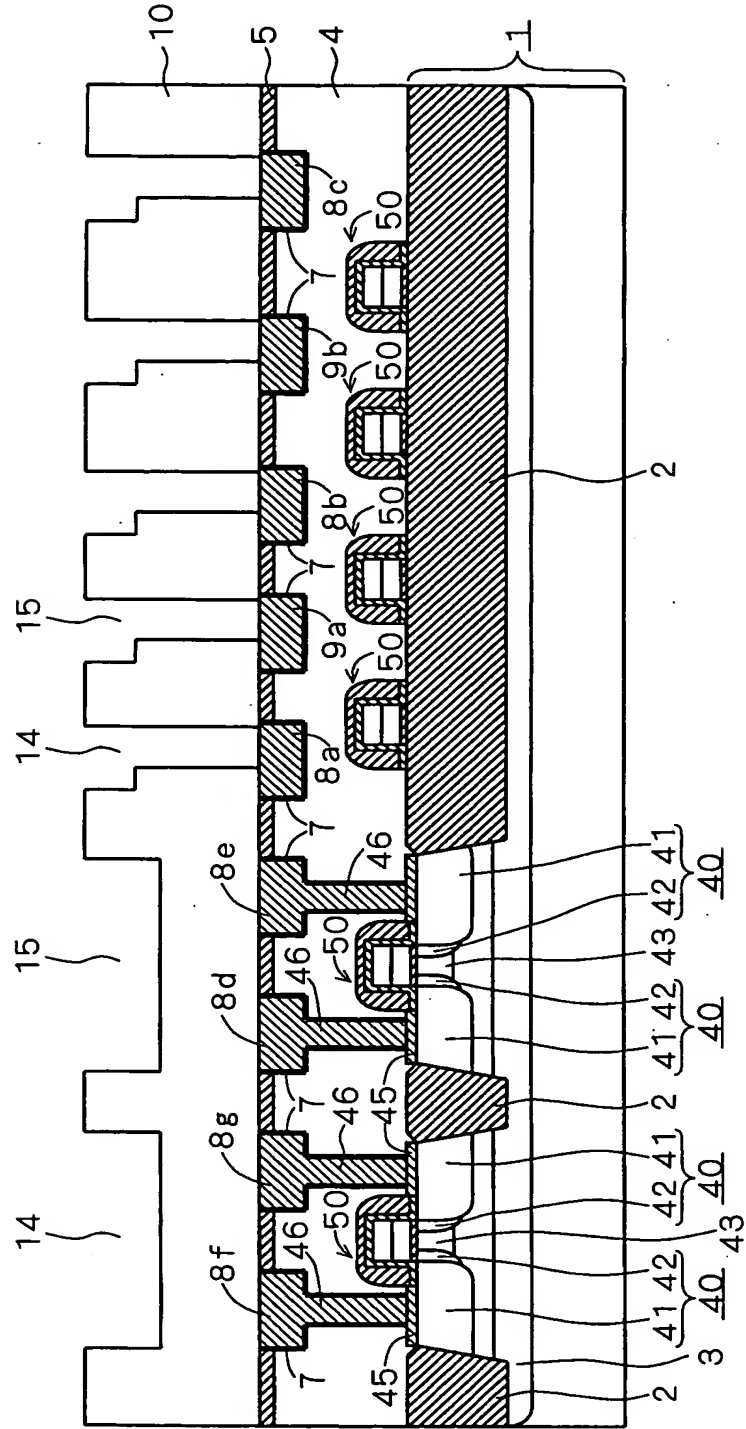


FIG. 4



F/G. 5

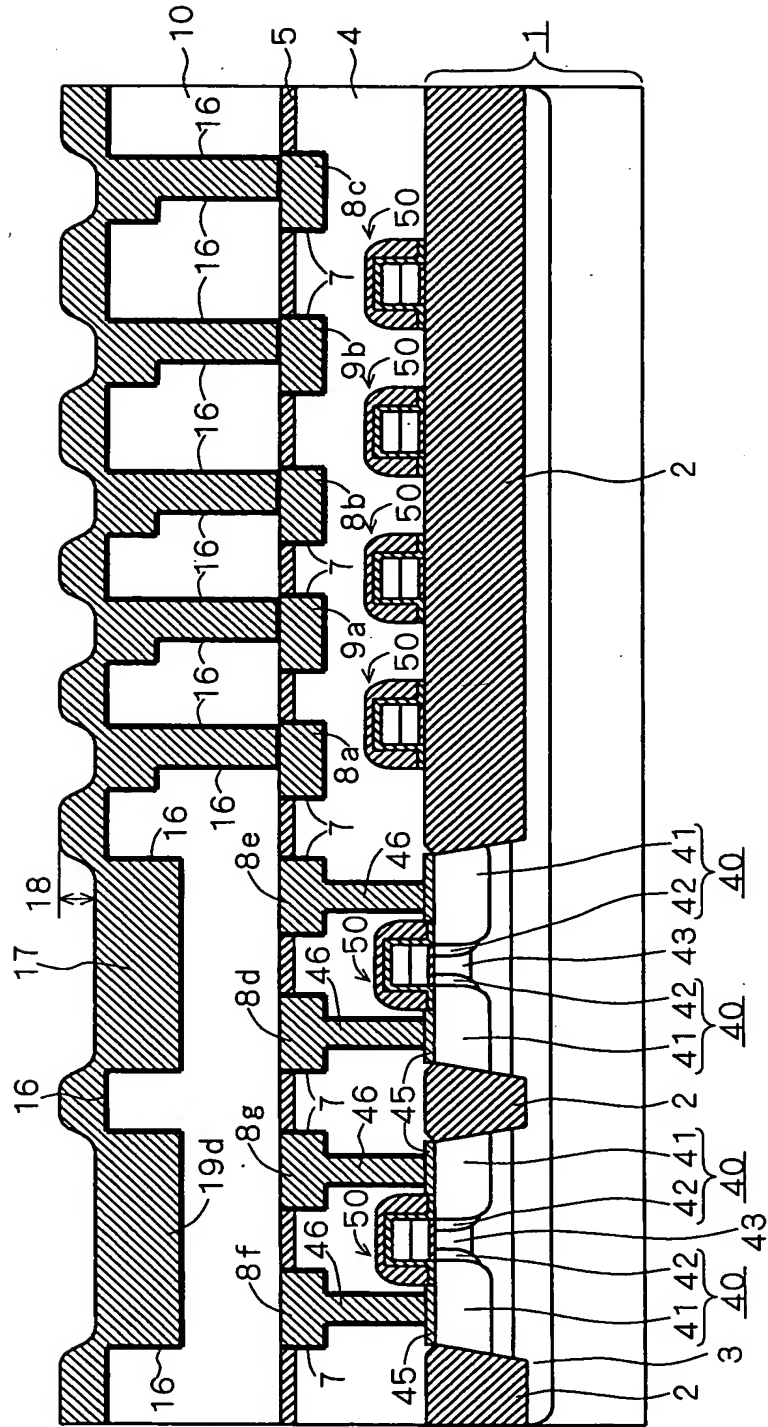


FIG. 6

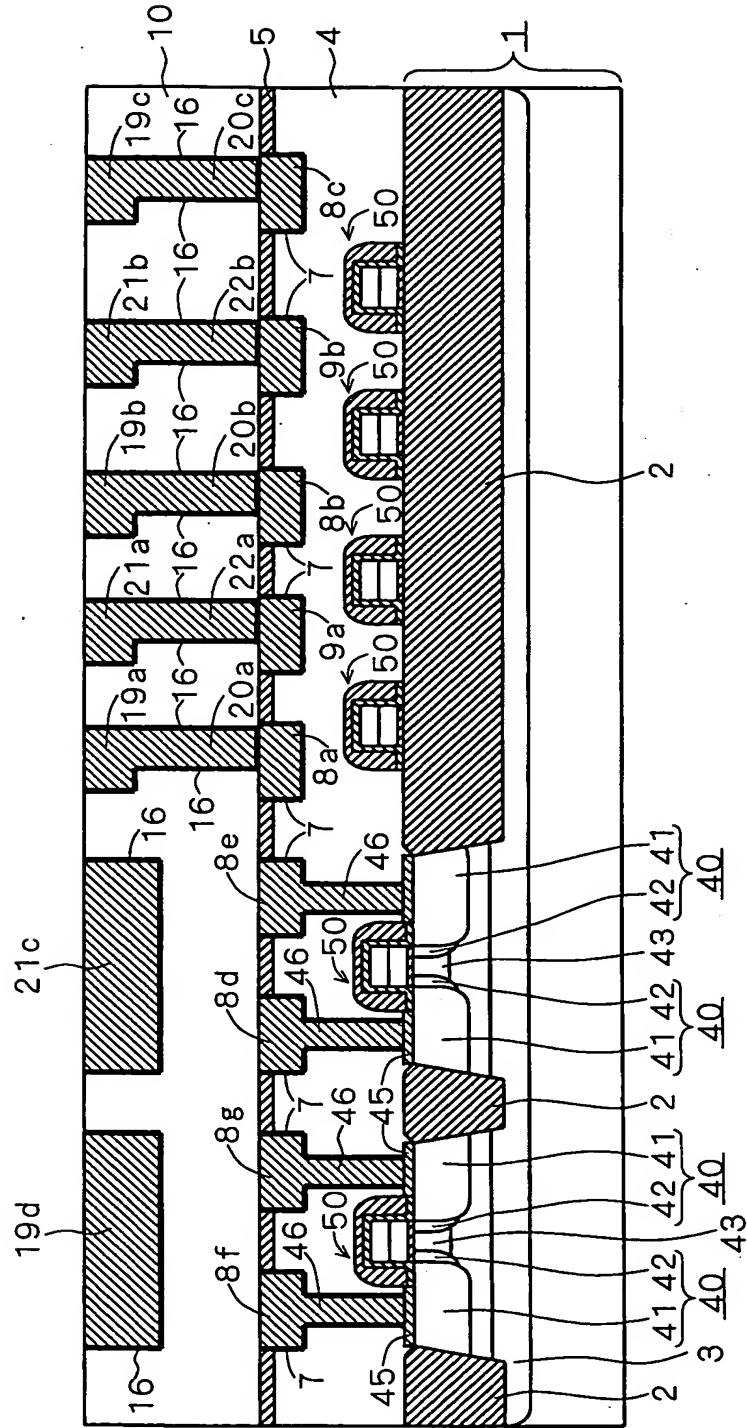


FIG. 7

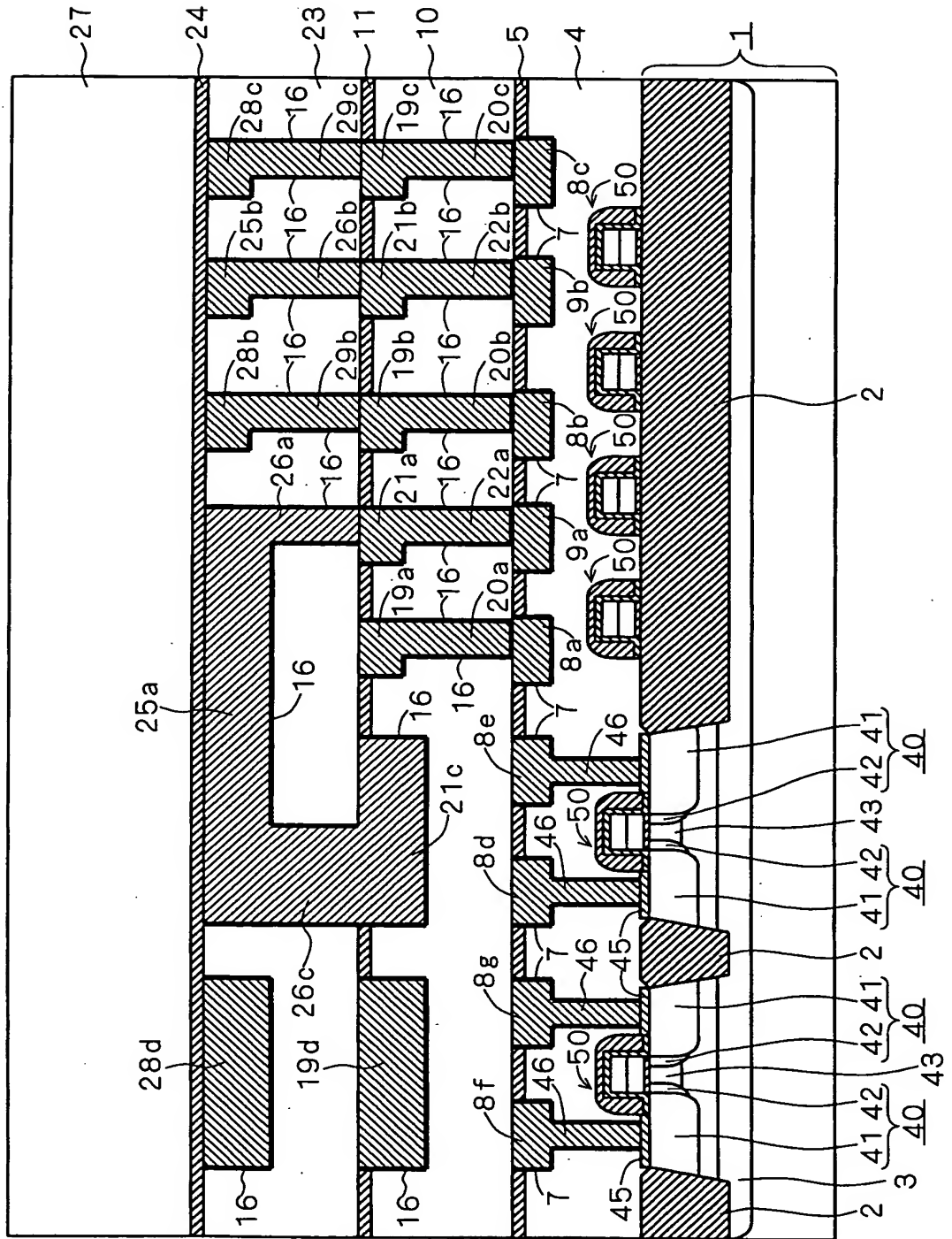


FIG. 8

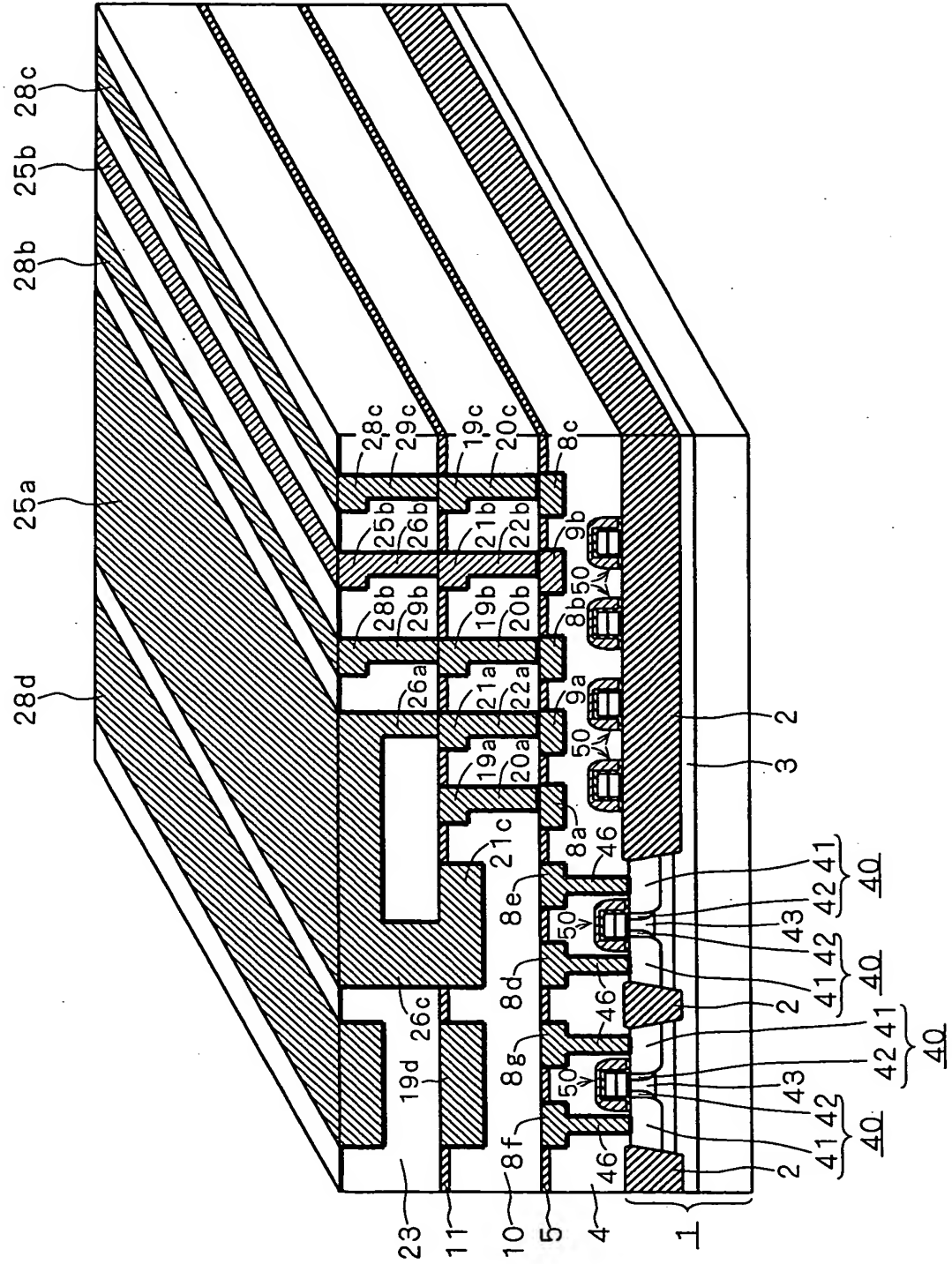


FIG. 9

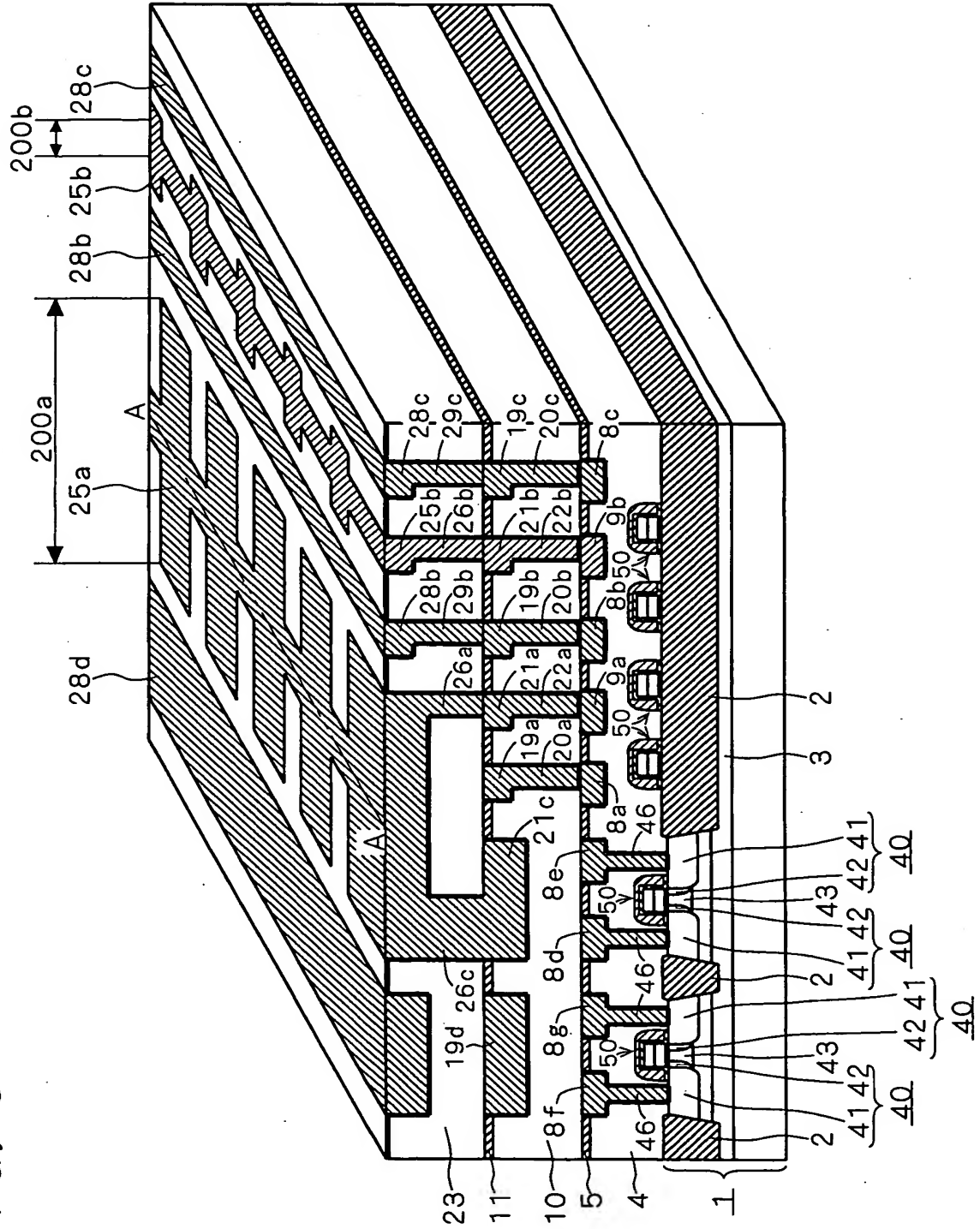


FIG. 10

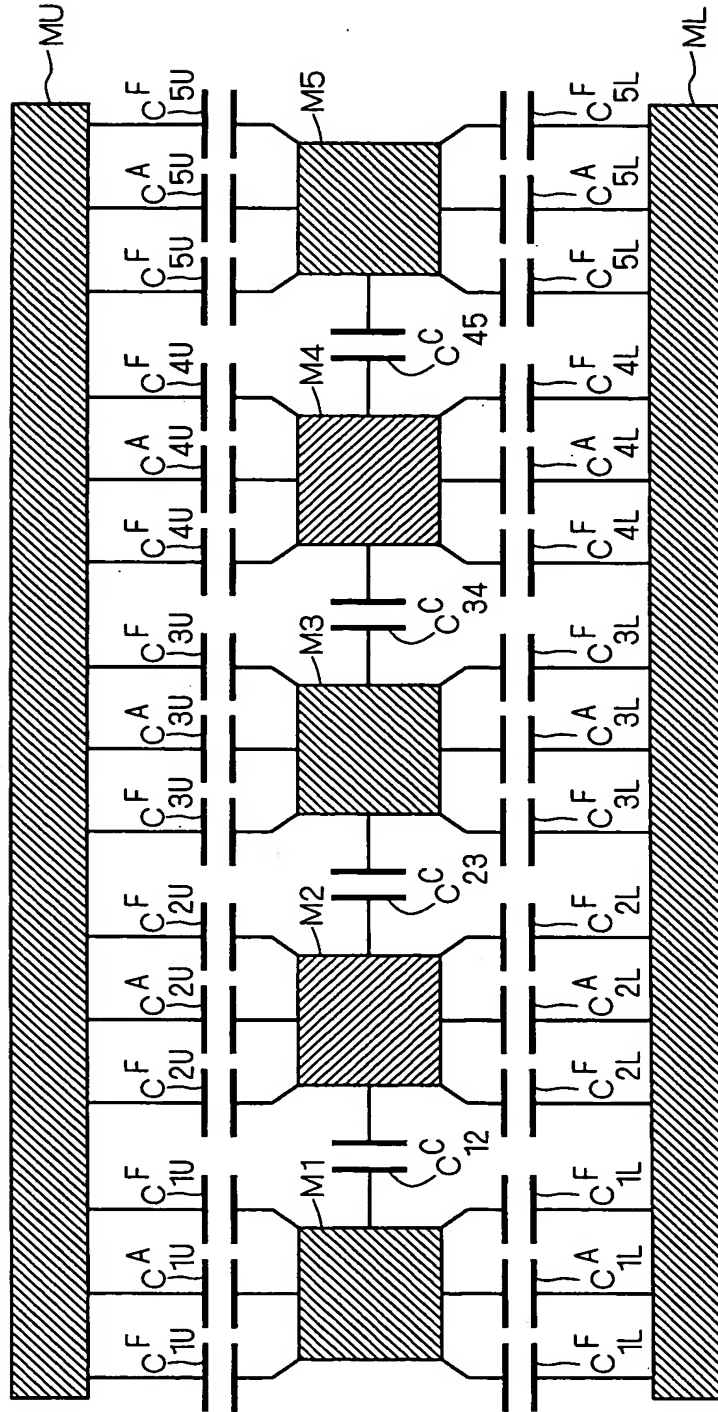


FIG. 11

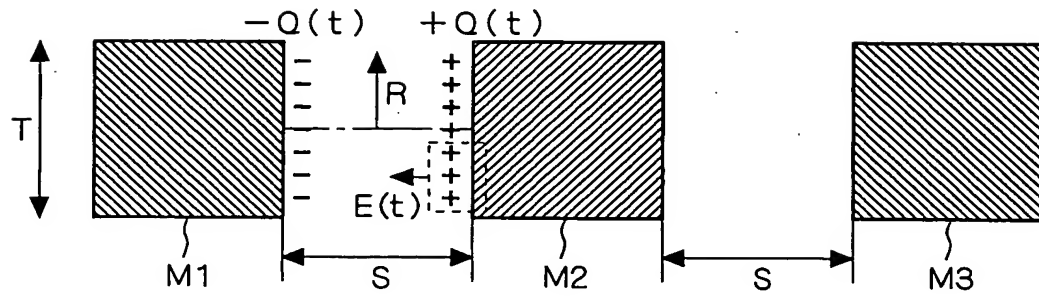


FIG. 12

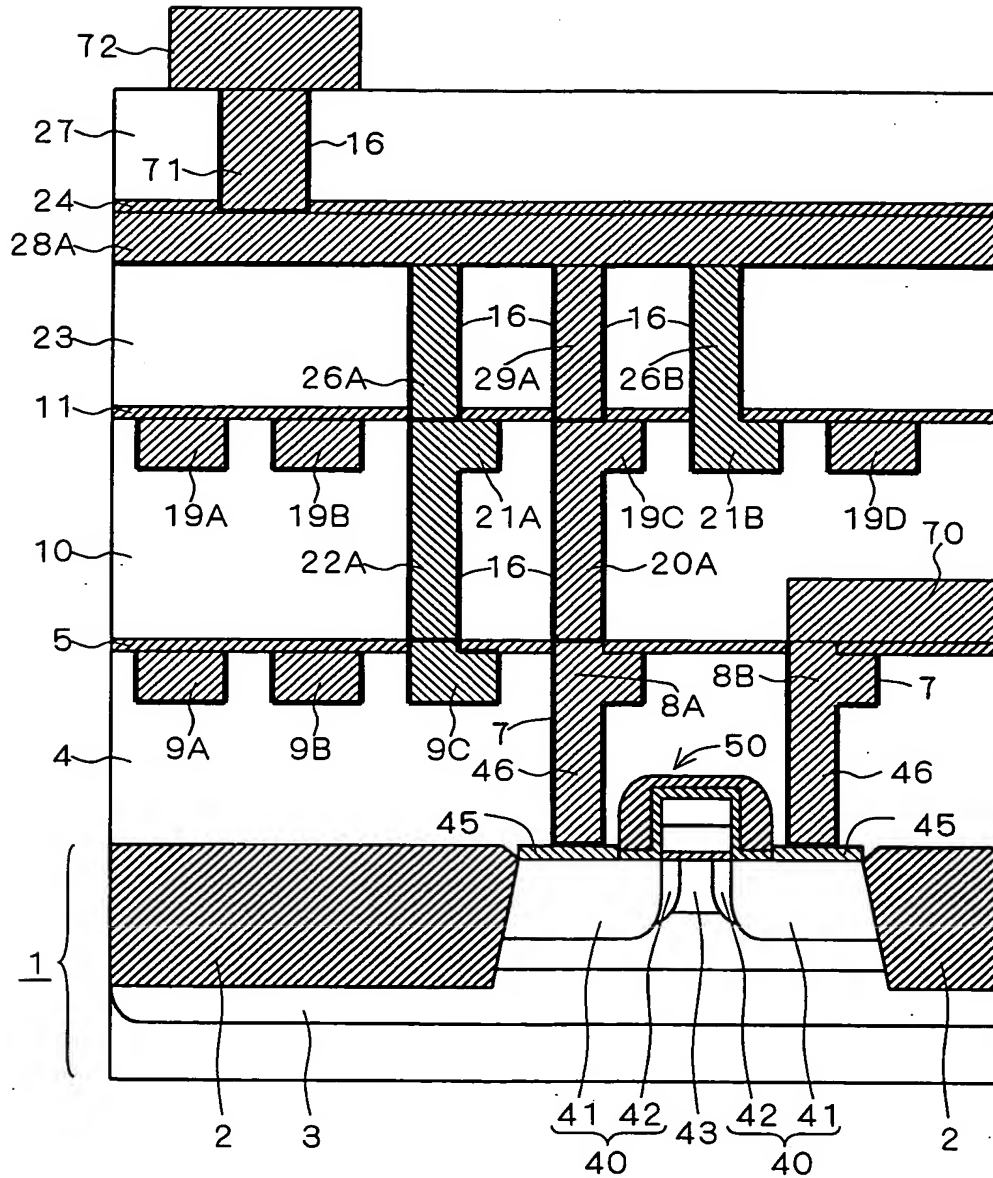


FIG. 13

	INTERCONNECTION 19C	DUMMY INTERCONNECTIONS 21A, 21B
1	VDD	VDD
2	VDD	VSS
3	VDD	VBB
4	VPC	VPC
5	VPC	VSS
6	VPC	VBB
7	VSS	VDD
8	VSS	VSS
9	VSS	VBB
10	VBB	VDD
11	VBB	VSS
12	VBB	VBB
13	VSIG	VDD
14	VSIG	VPC
15	VSIG	VSS
16	VSIG	VBB

[illegible]

FIG. 15

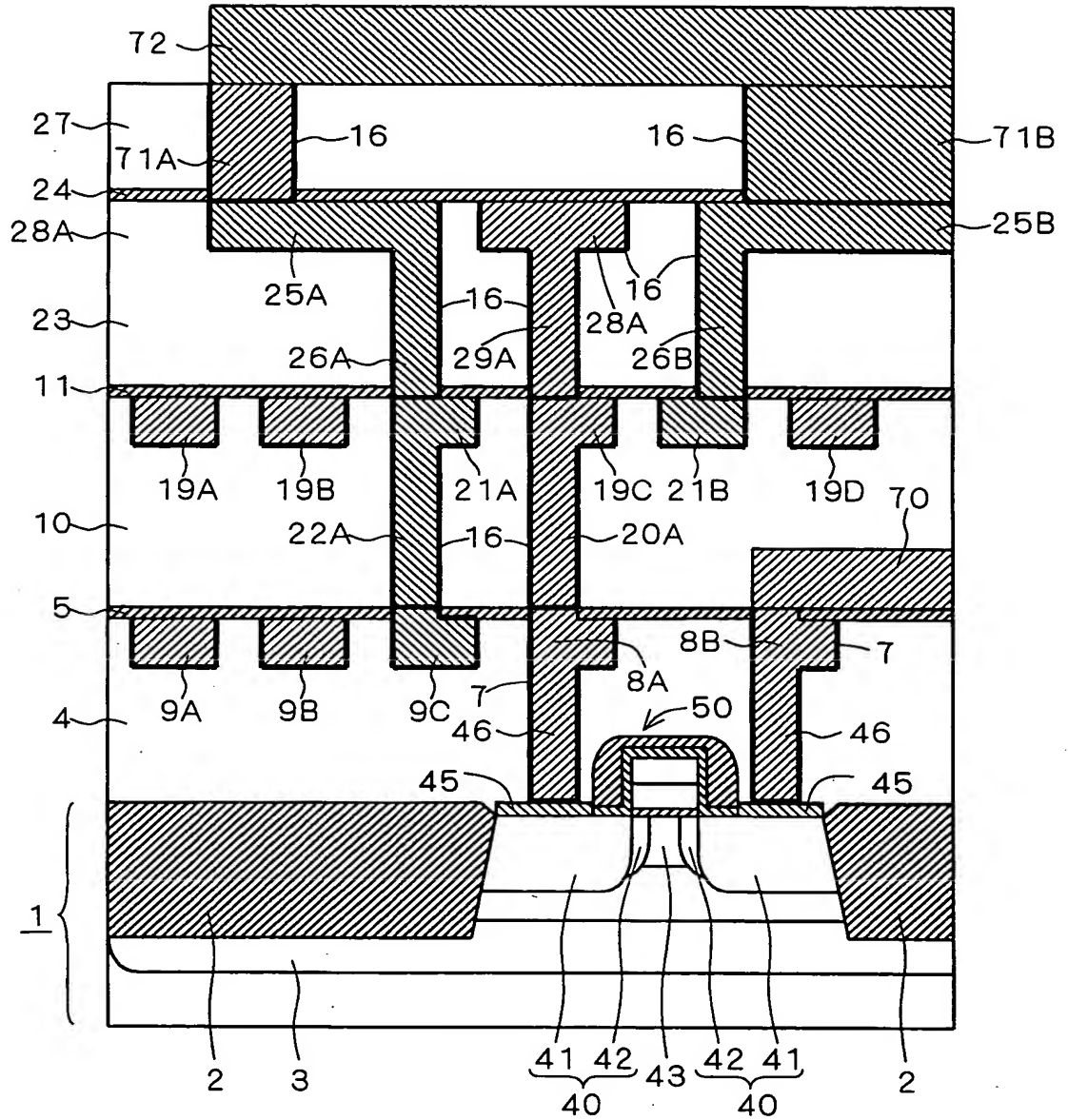


FIG. 16

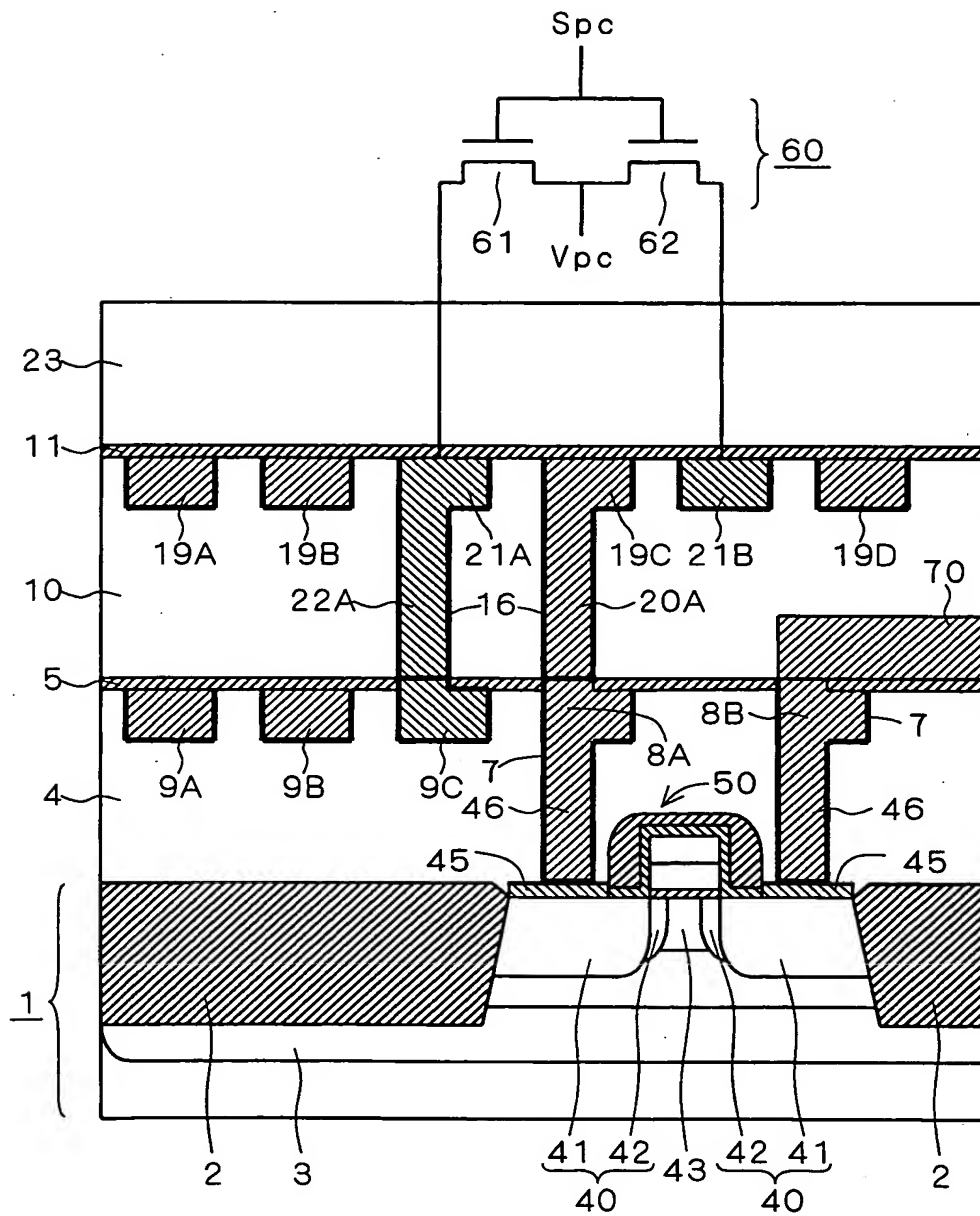


FIG. 17

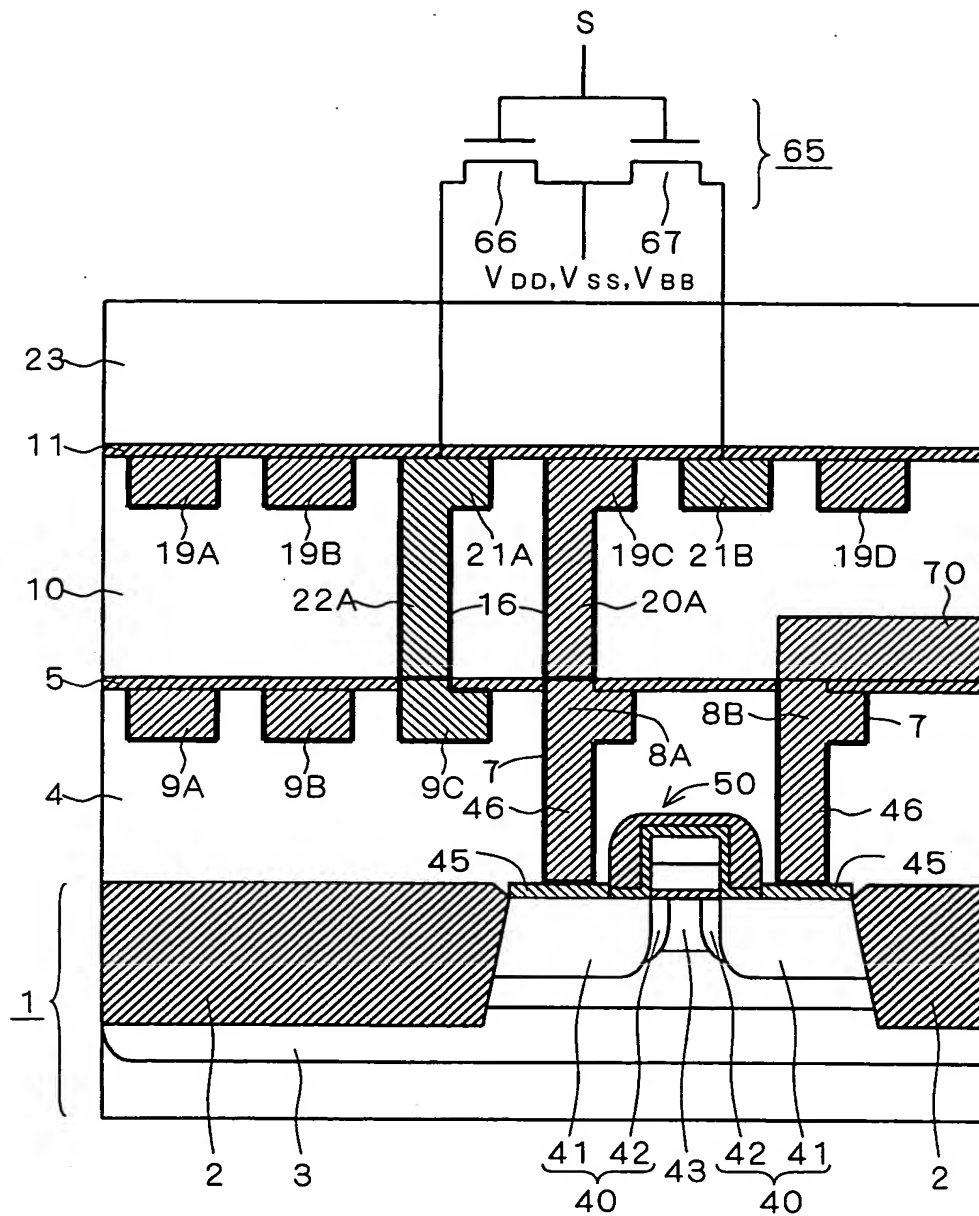


FIG. 18

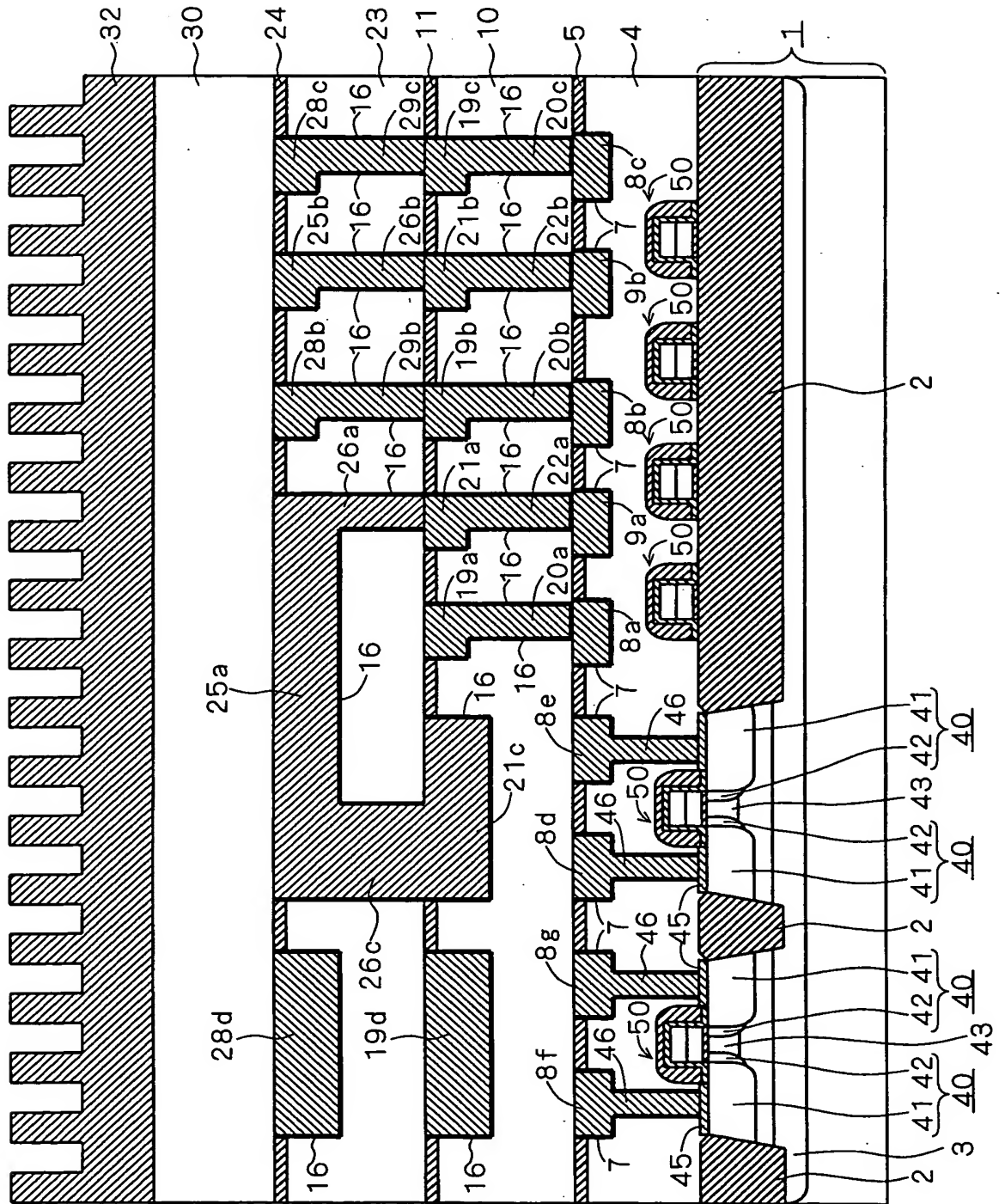


FIG. 19

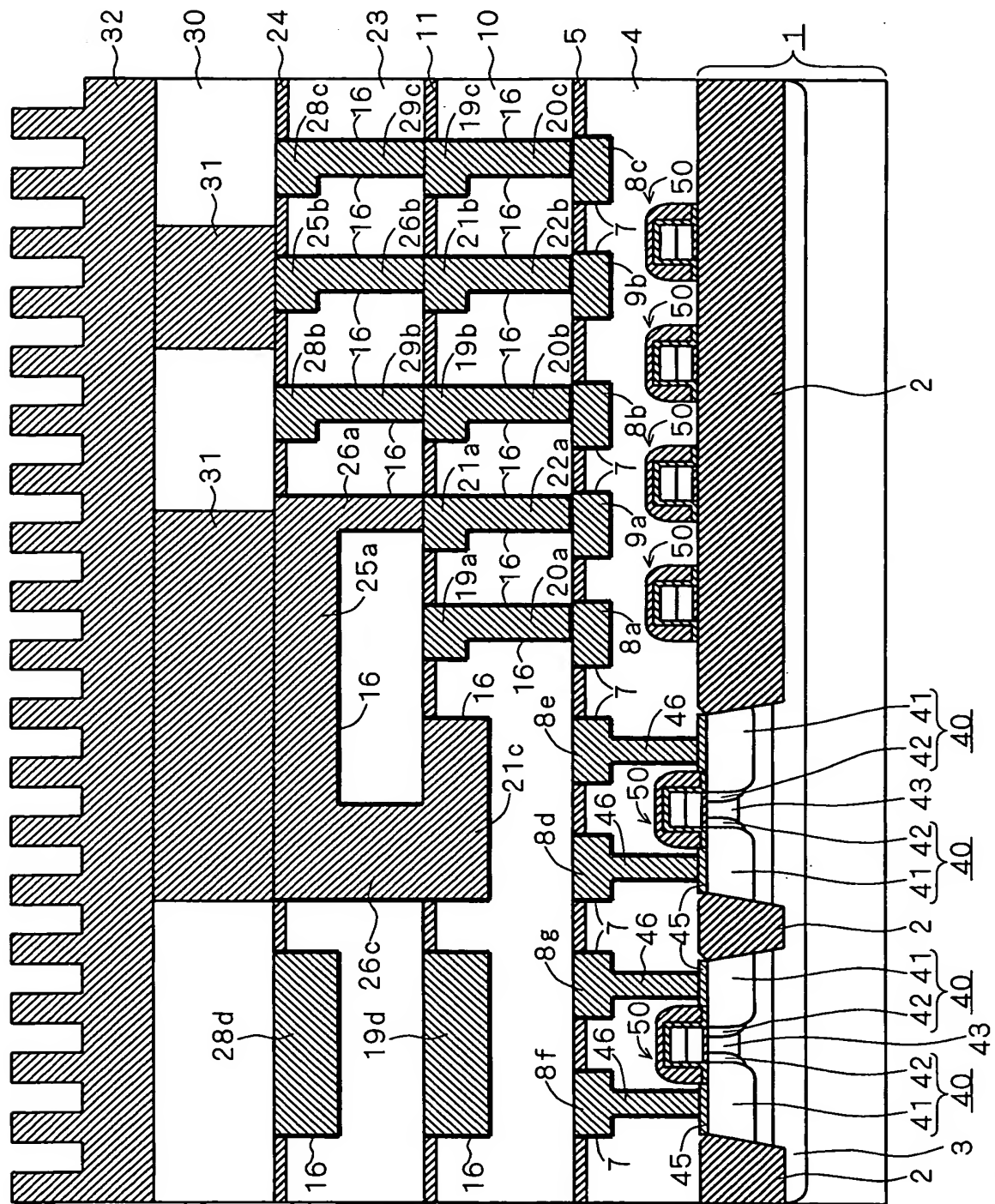


FIG. 20

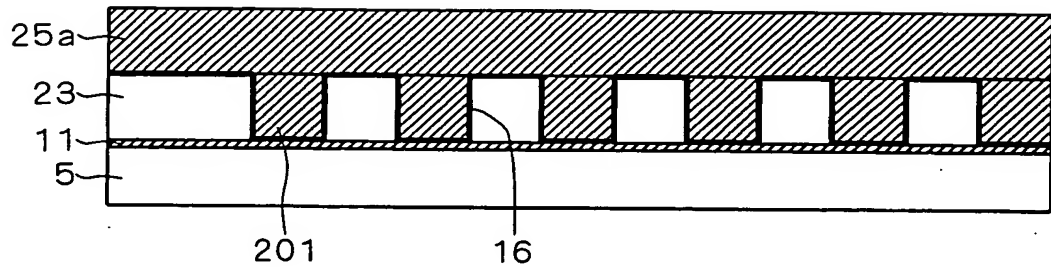


FIG. 21

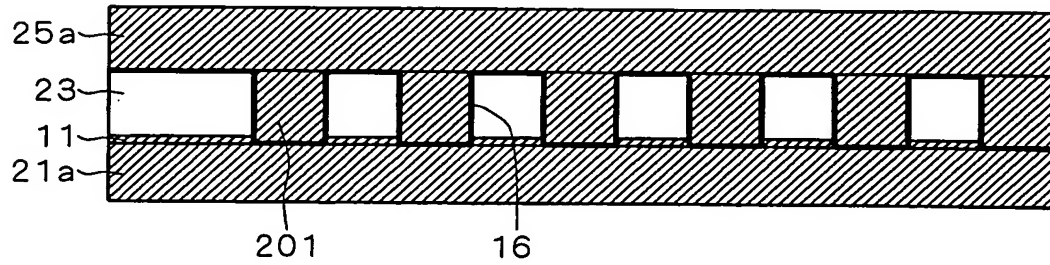


FIG. 22

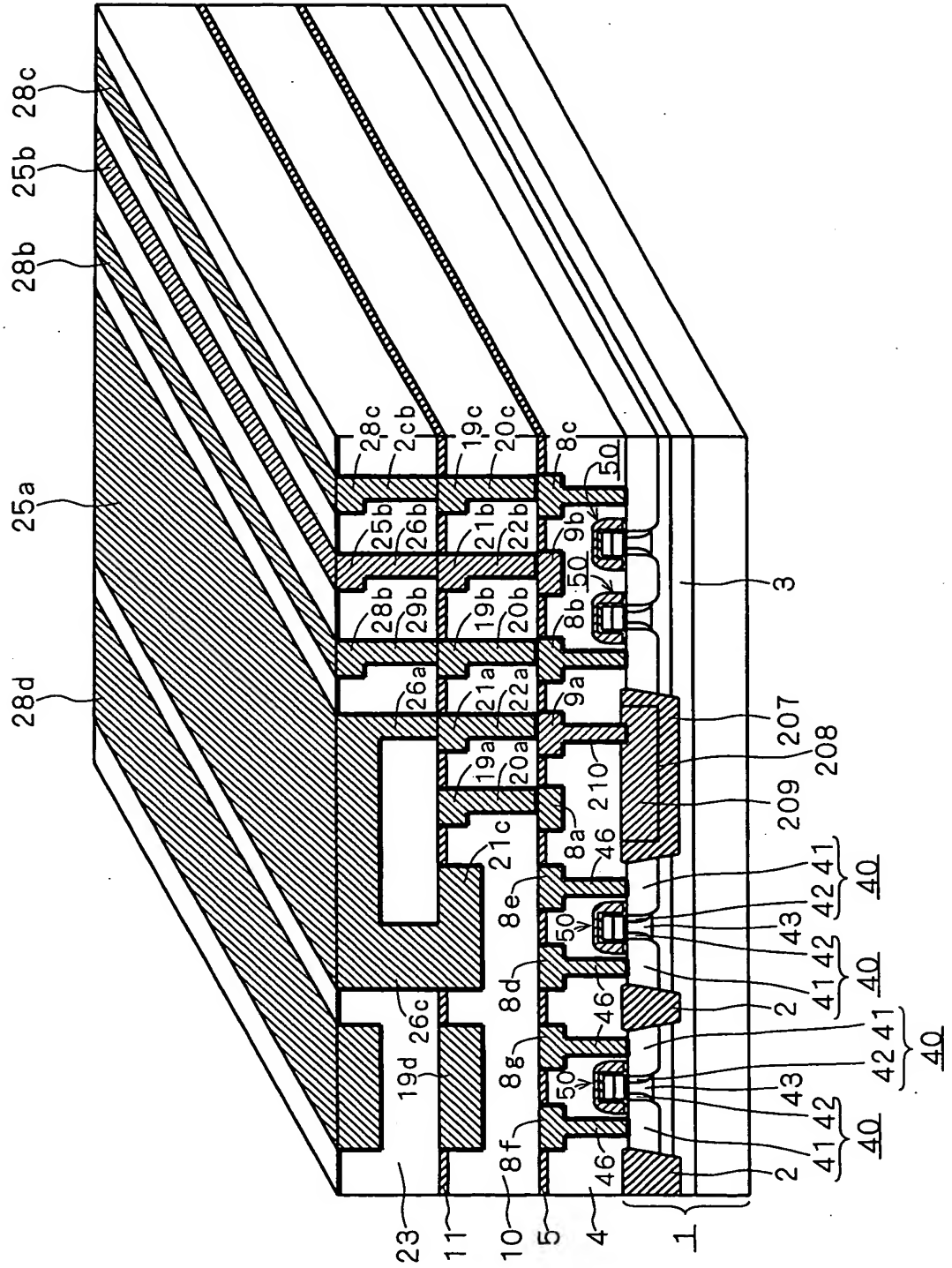


FIG. 23

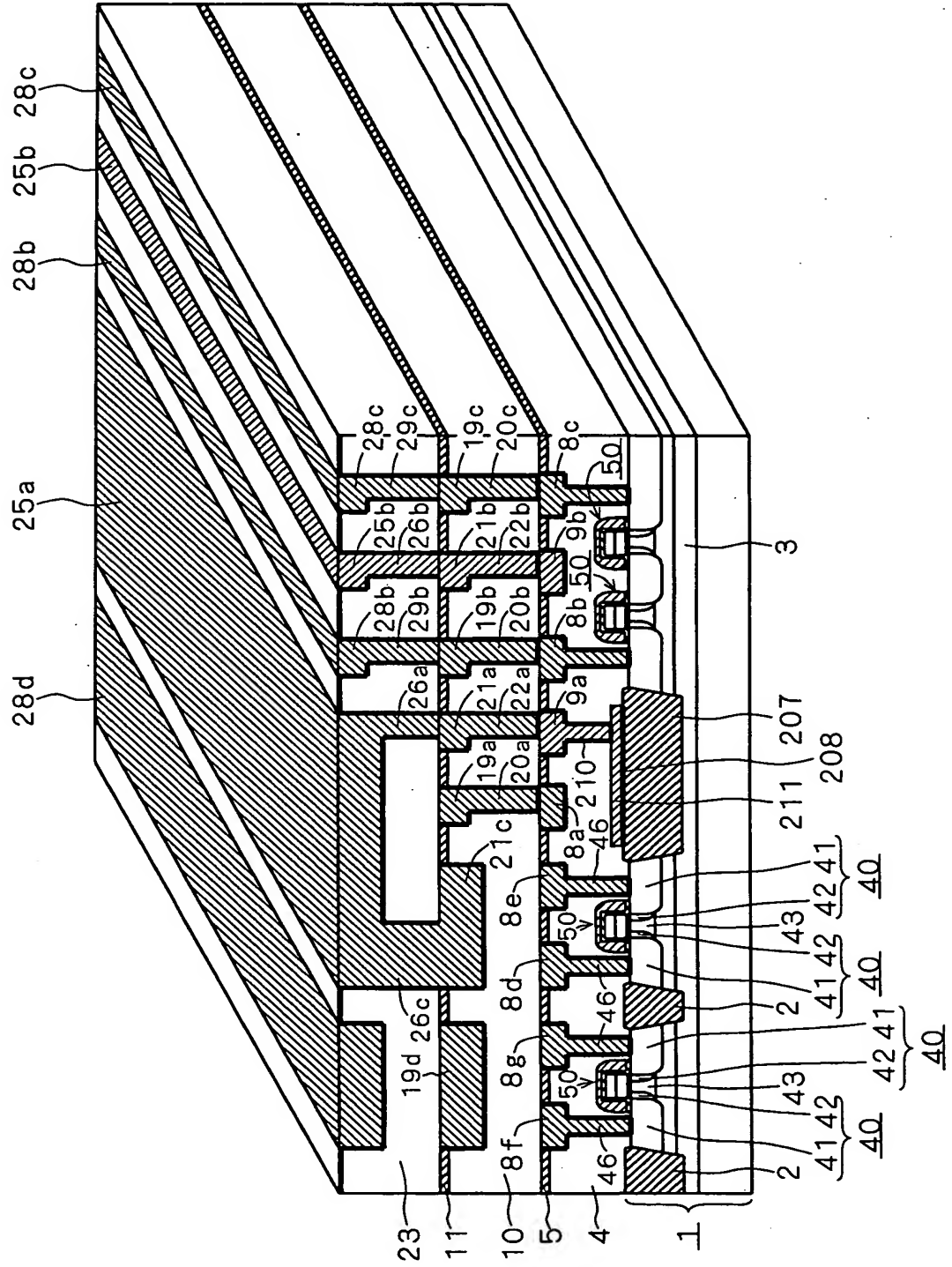


FIG. 24

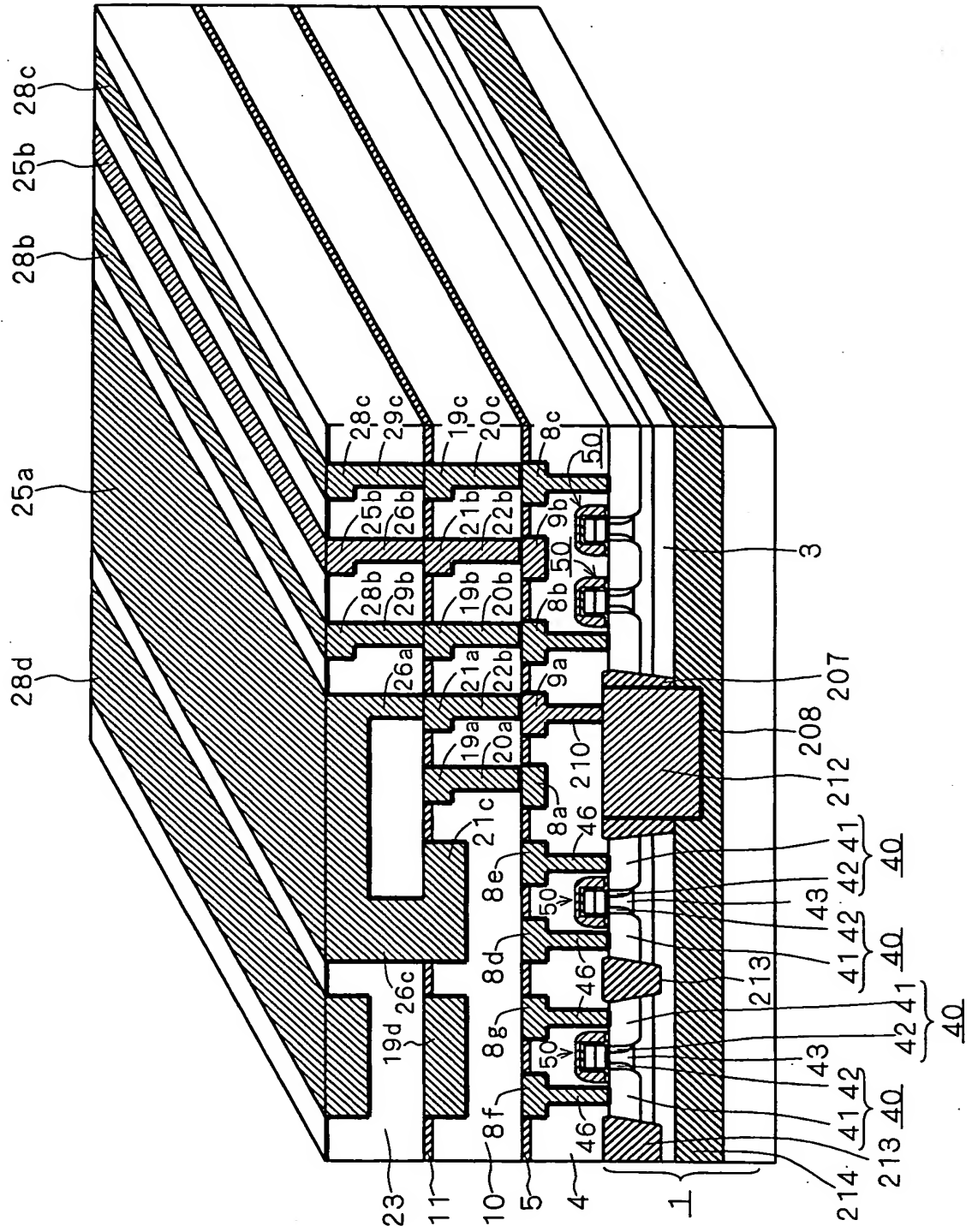


FIG. 25

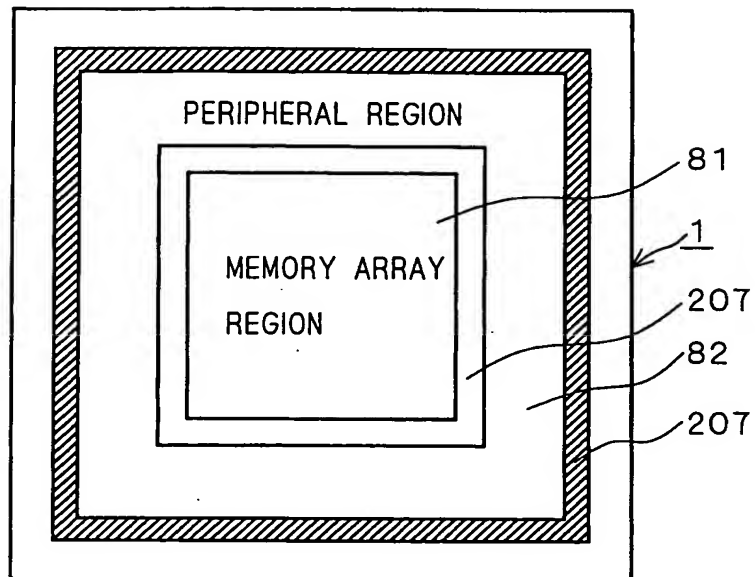
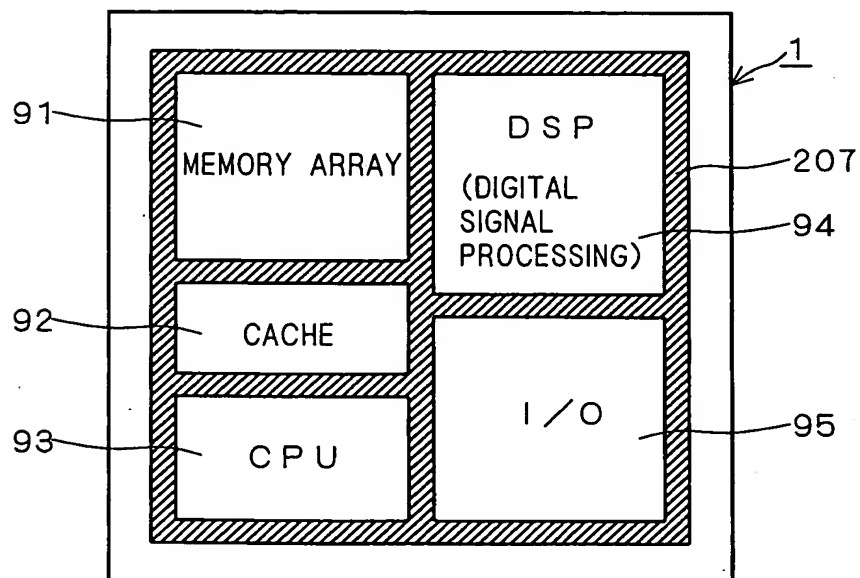
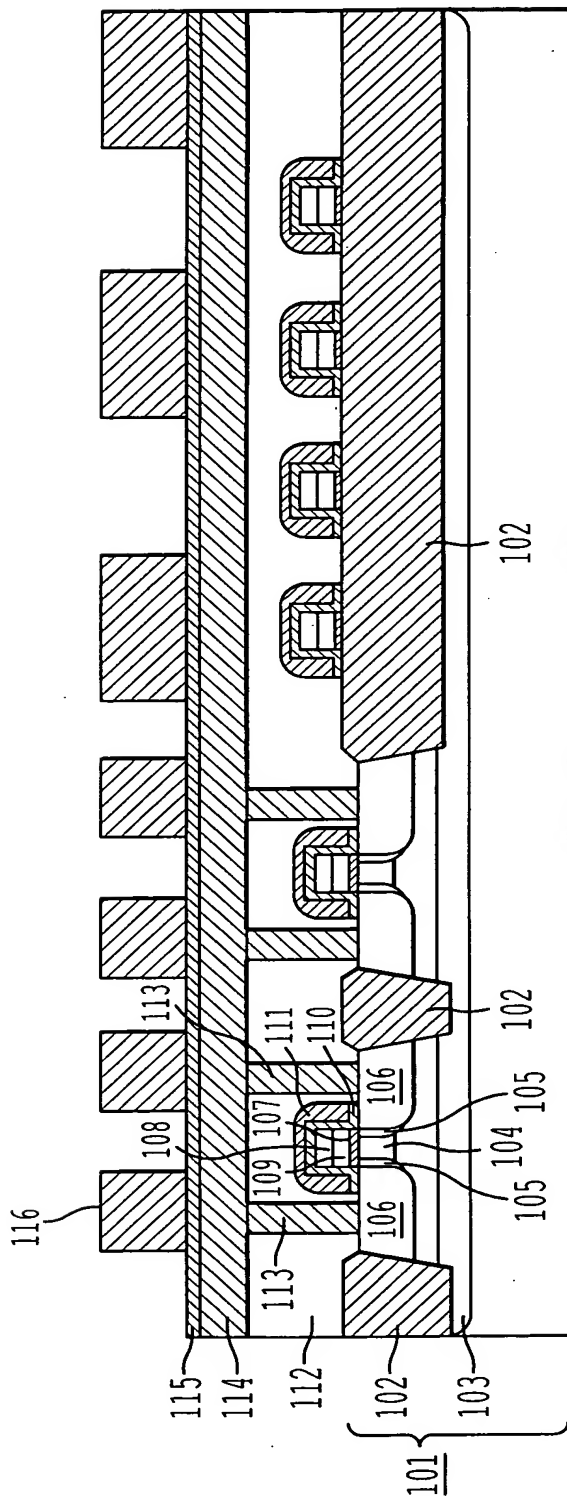


FIG. 26





**FIG. 27**  
**PRIOR ART**

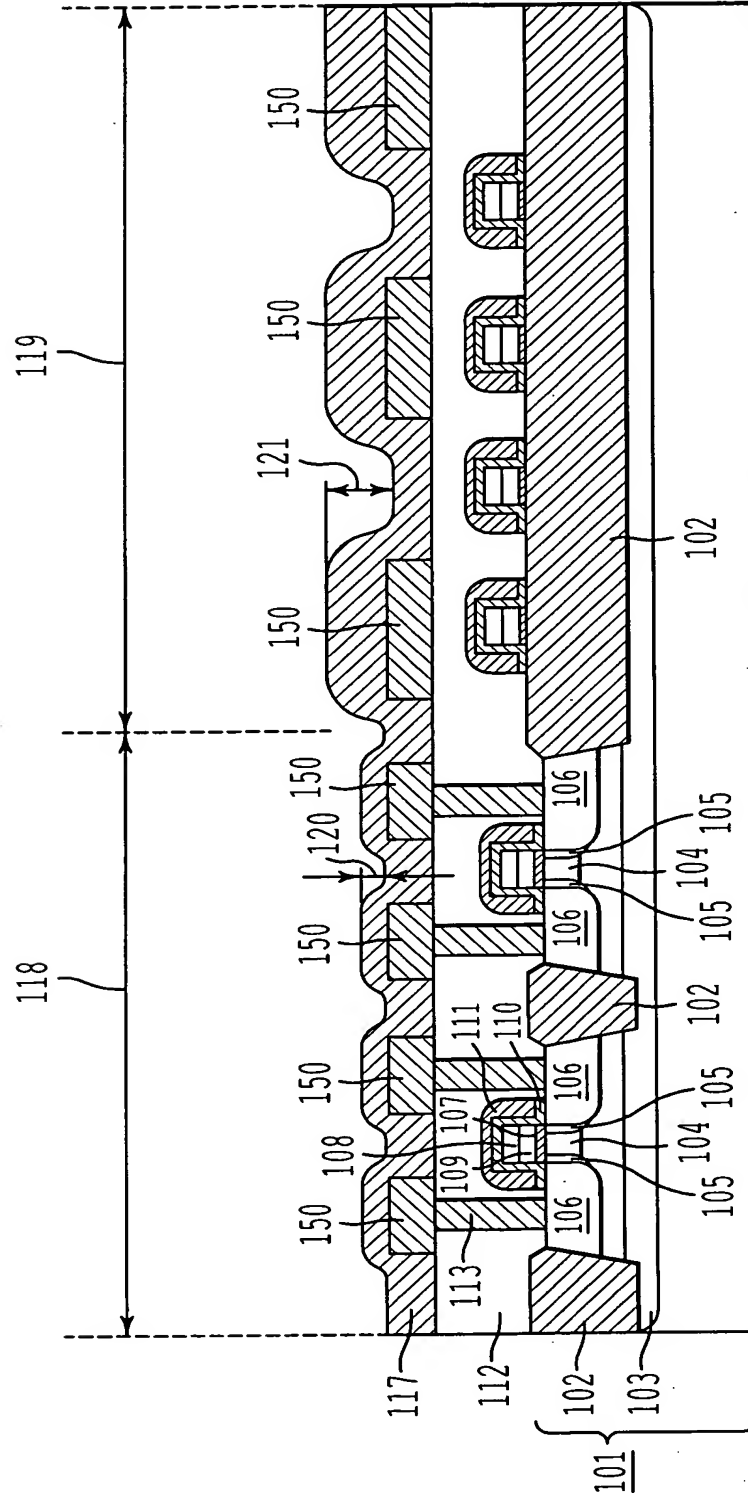
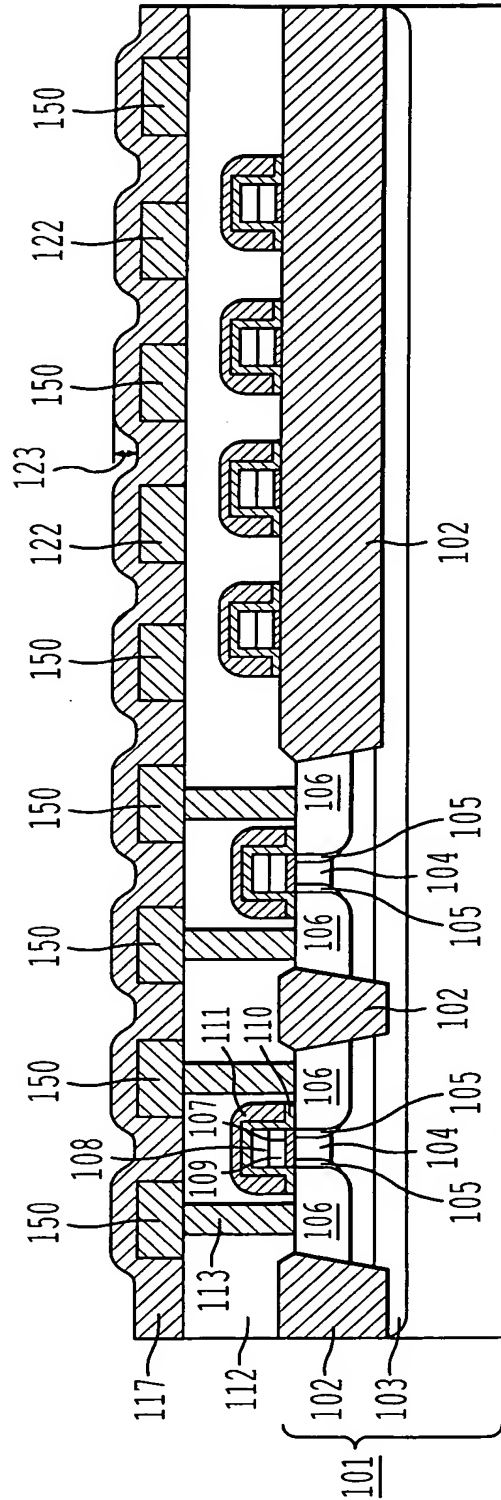
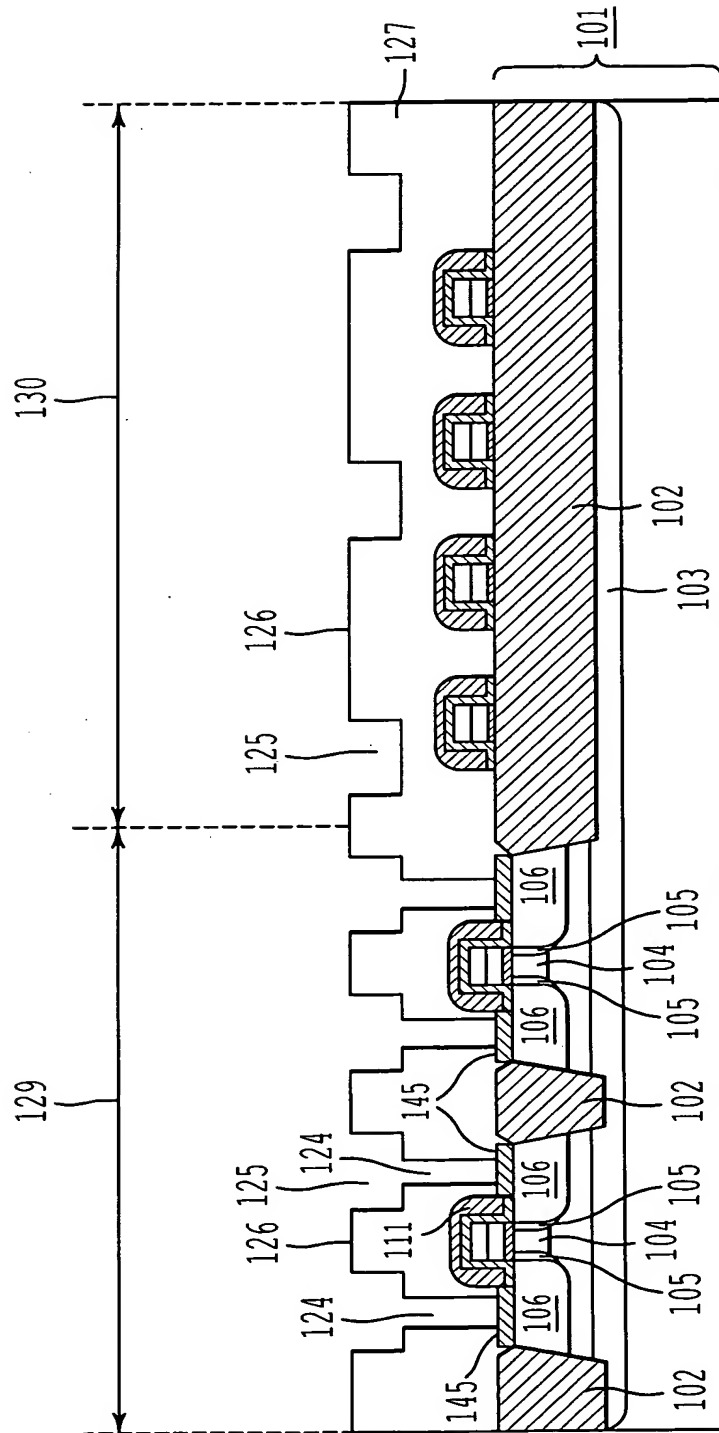


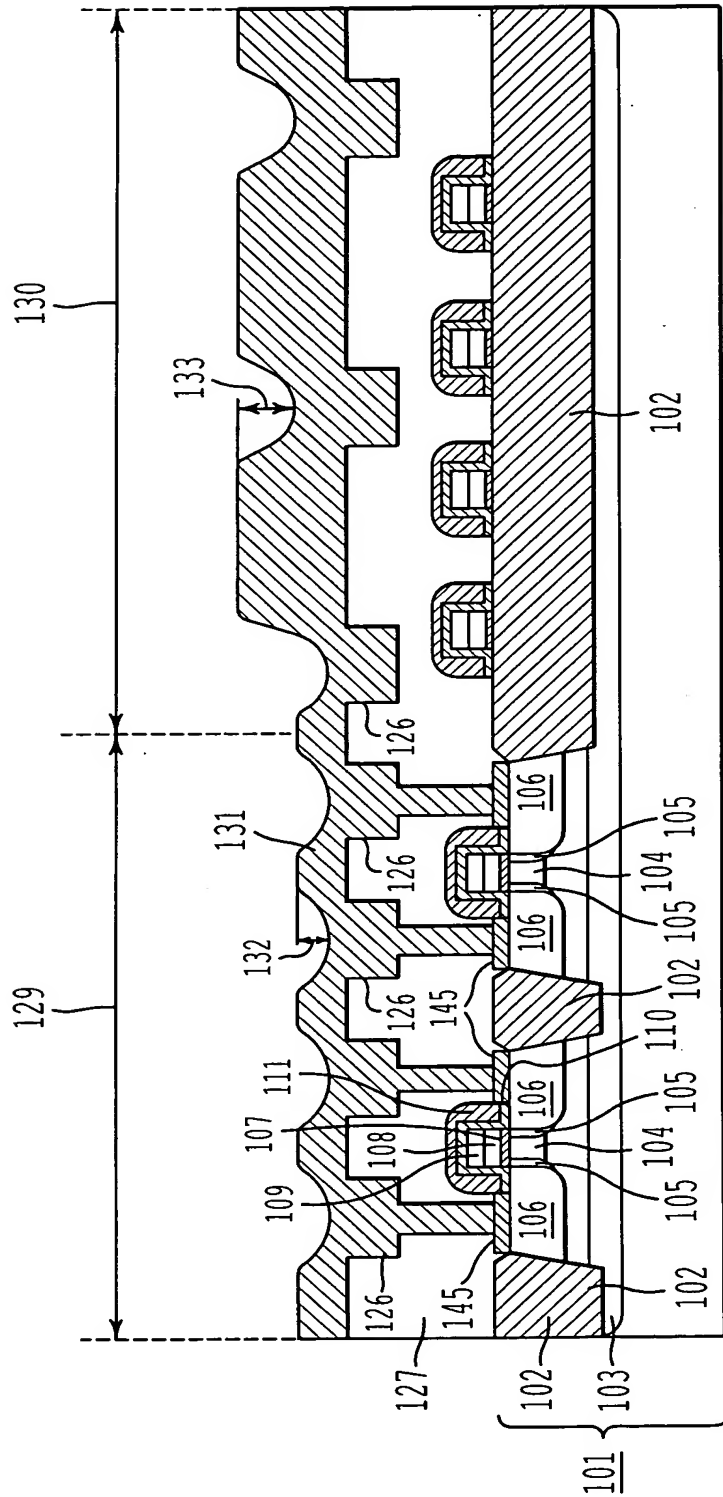
FIG. 28  
PRIOR ART



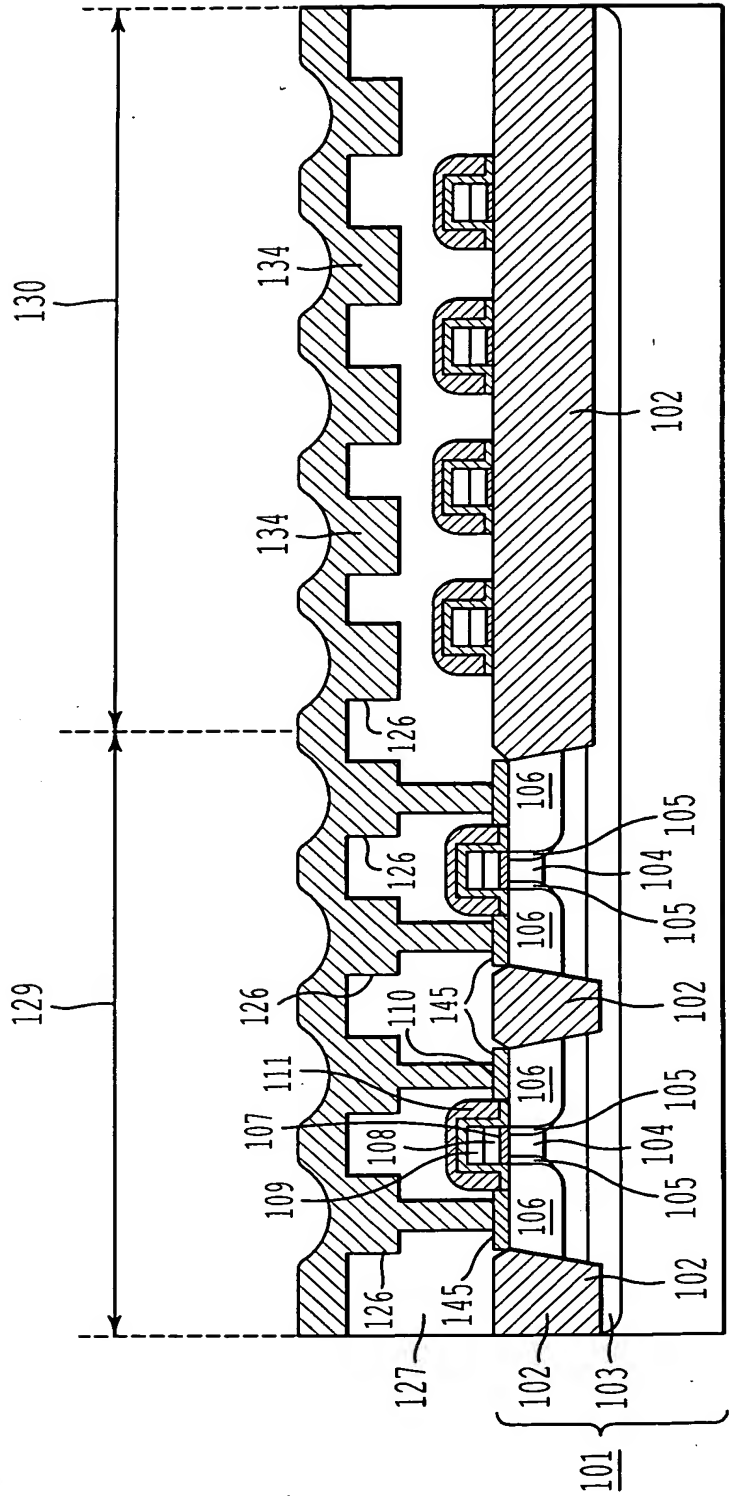
**FIG. 29**  
**PRIOR ART**



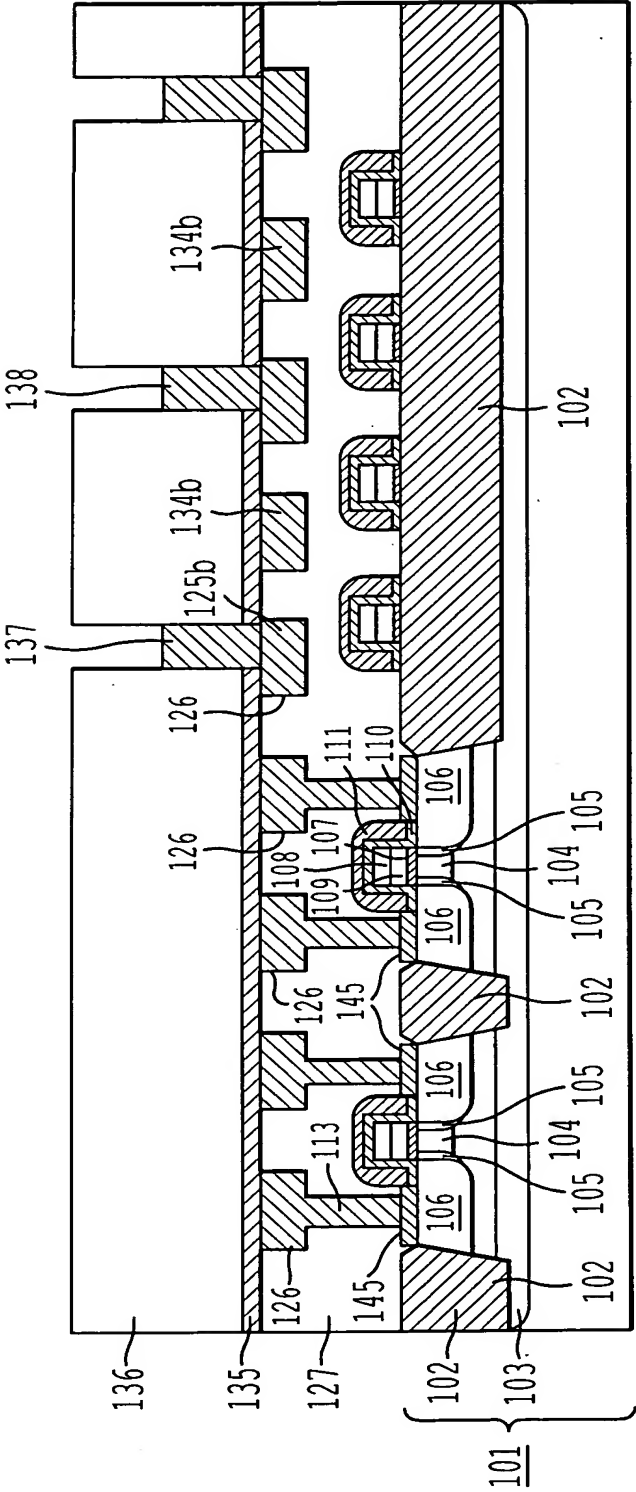
**FIG. 30**  
**PRIOR ART**



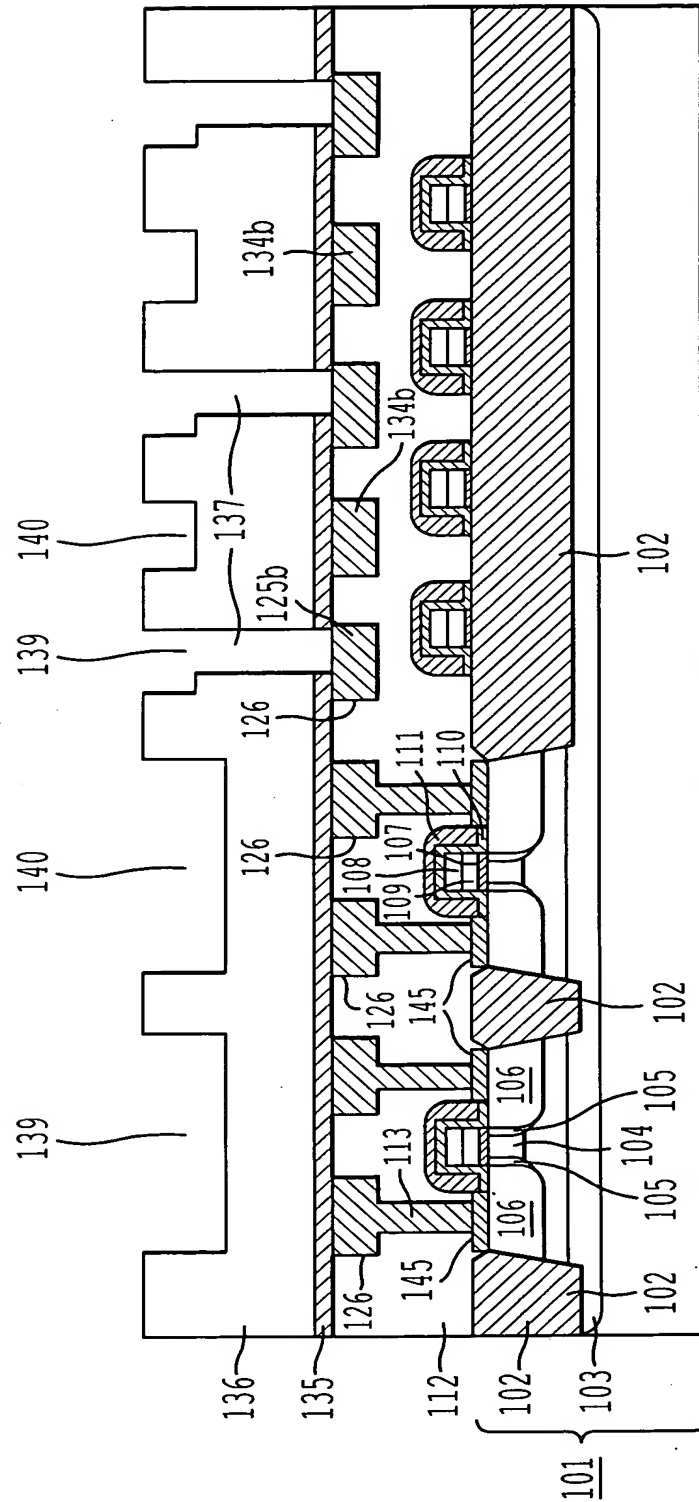
*FIG. 31*  
*PRIOR ART*



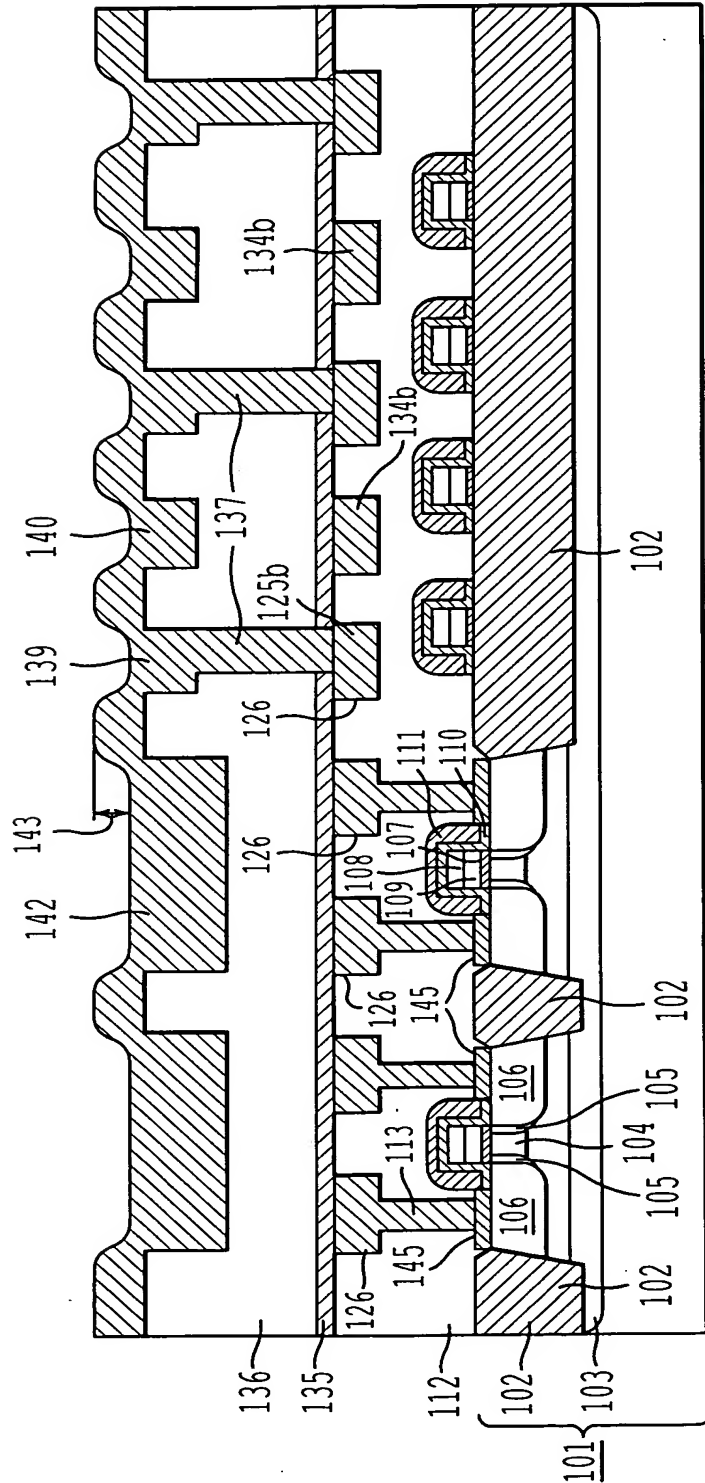
*FIG. 32*  
*PRIOR ART*



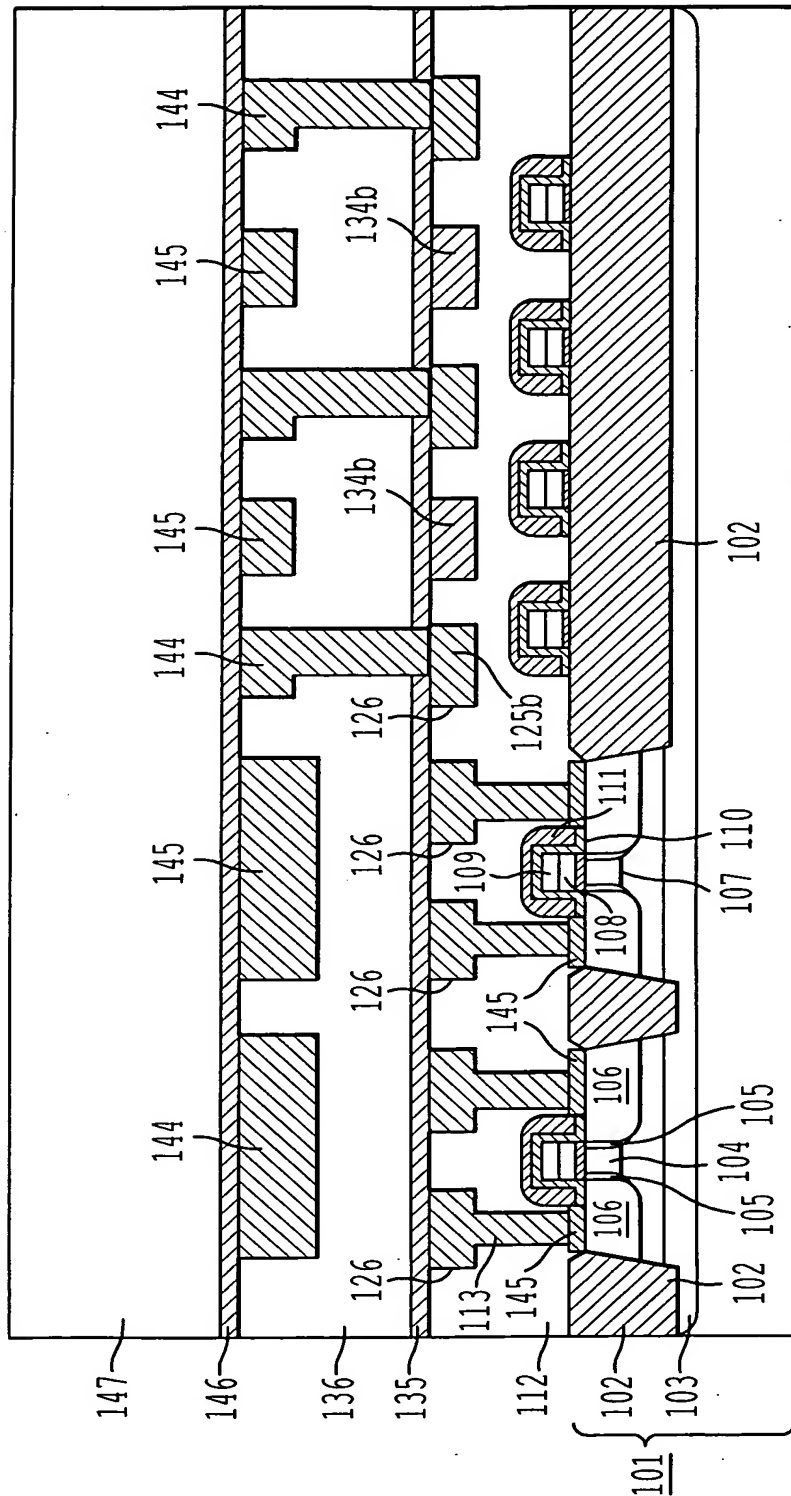
*FIG. 33*  
*PRIOR ART*



**FIG. 34**  
**PRIOR ART**



**FIG. 35**  
**PRIOR ART**



**FIG. 36**  
**PRIOR ART**